Status of the new LLRF for ASTRID and ASTRID2

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ASTRID2

- ASTRID2 is the new synchrotron light source being built in Århus, Denmark
- ASTRID2 main parameters
  - Electron energy: 580 MeV
  - Emittance: 12 nm
  - Beam Current: 200 mA
  - Circumference: 45.7 m
  - 6-fold symmetry
    - lattice: DBA with 12 combined function dipole magnets
      - Integrated quadrupole gradient
  - 4 straight sections for insertion devices
  - Will use ASTRID as booster (full energy injection)
    - Allows top-up operation

ASTRID2 Layout

ASTRID2 Status

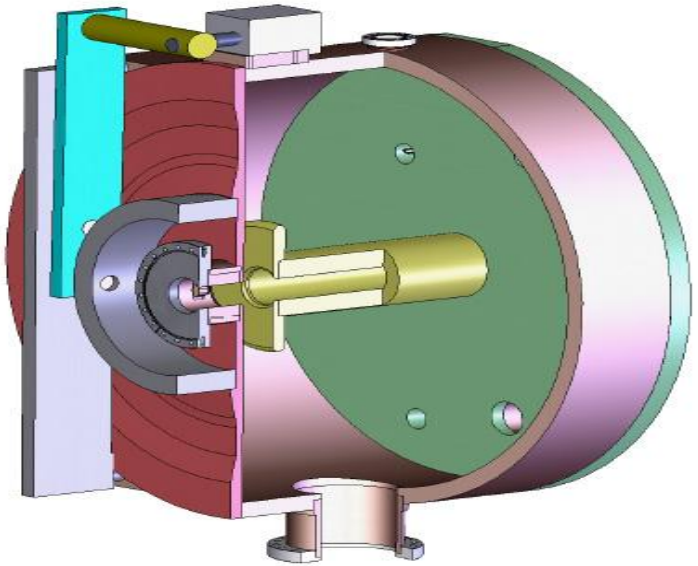
- Most major components, except RF cavity, will be delivered Jan. 2011
  - magnets on girders, fast magnets, magnet power supplies
- Vacuum chamber is being finalized
- Timeline
  - 2011: Installation and commission synchrotron
  - 2012: First beamlines on ASTRID2
  - 2013: All beamlines transferred to ASTRID2

ASTRID2 RF

- 105 MHz (like ASTRID)
- Main RF parameters
  - Harmonic: 16
  - RF voltage: 50–200 kV
  - Synchrotron frequency: 10–20 kHz
  - Synchrotron radiation power: ~1.4 kW
  - Cavity power: 0.8–12 kW
- 5–12 kW FM transmitter
  - Most likely a solid-state amplifier, but a tube-based amplifier is not ruled out

ASTRID2 Cavity

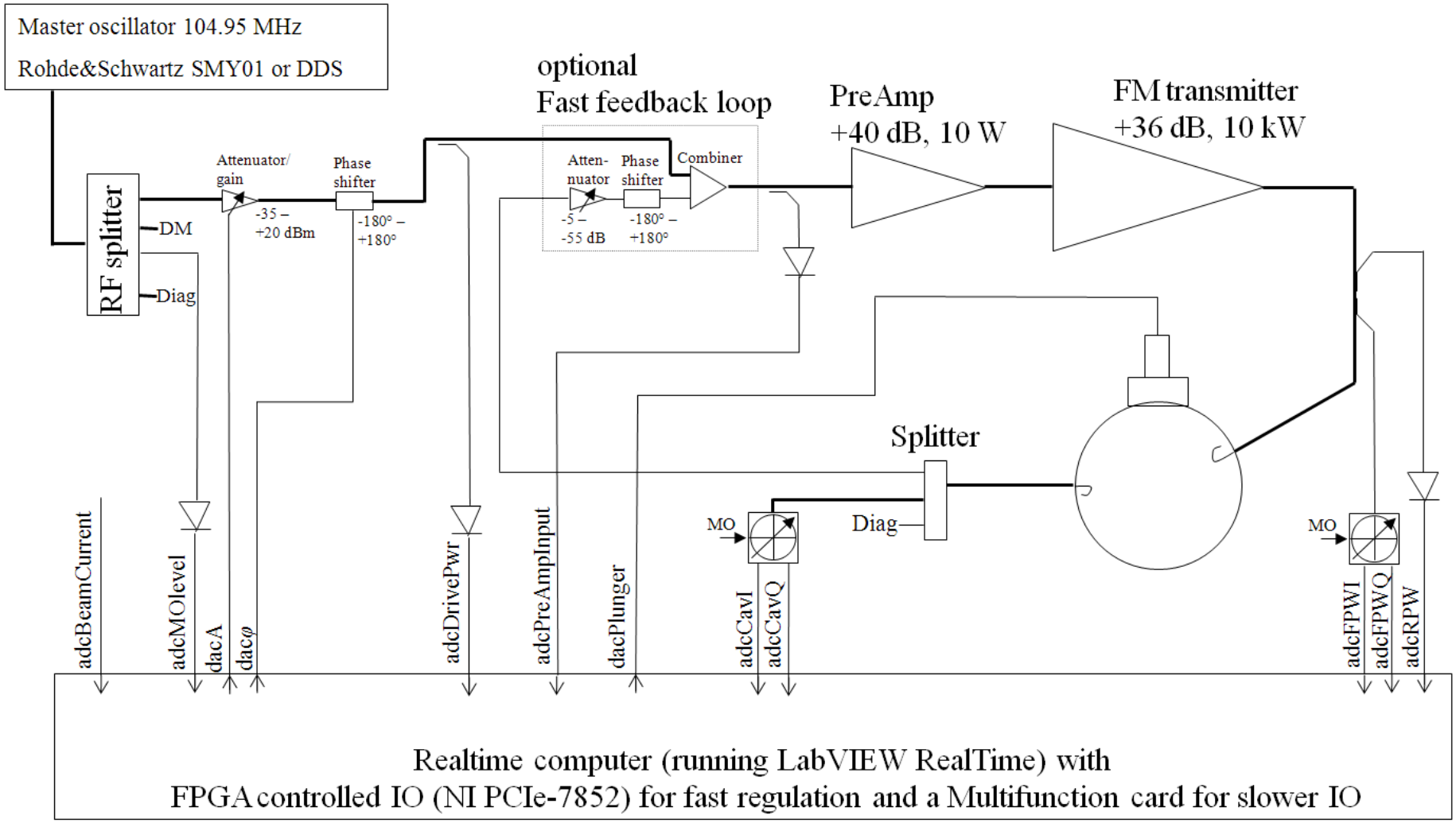
- Collaboration with MAX-lab
  - MAX-lab needs 8 cavities (100 MHz) for MAX IV
    - We need 2 cavities (105 MHz) (spare for ASTRID)
  - New MAX-lab cavity
    - Based on MAX II cavity
    - Use Electron Beam Welding instead of vacuum brazing
    - Have industry build after MAX-lab RF design
      - Tender: Soon
  - Expect to get a 315 MHz Landau cavity



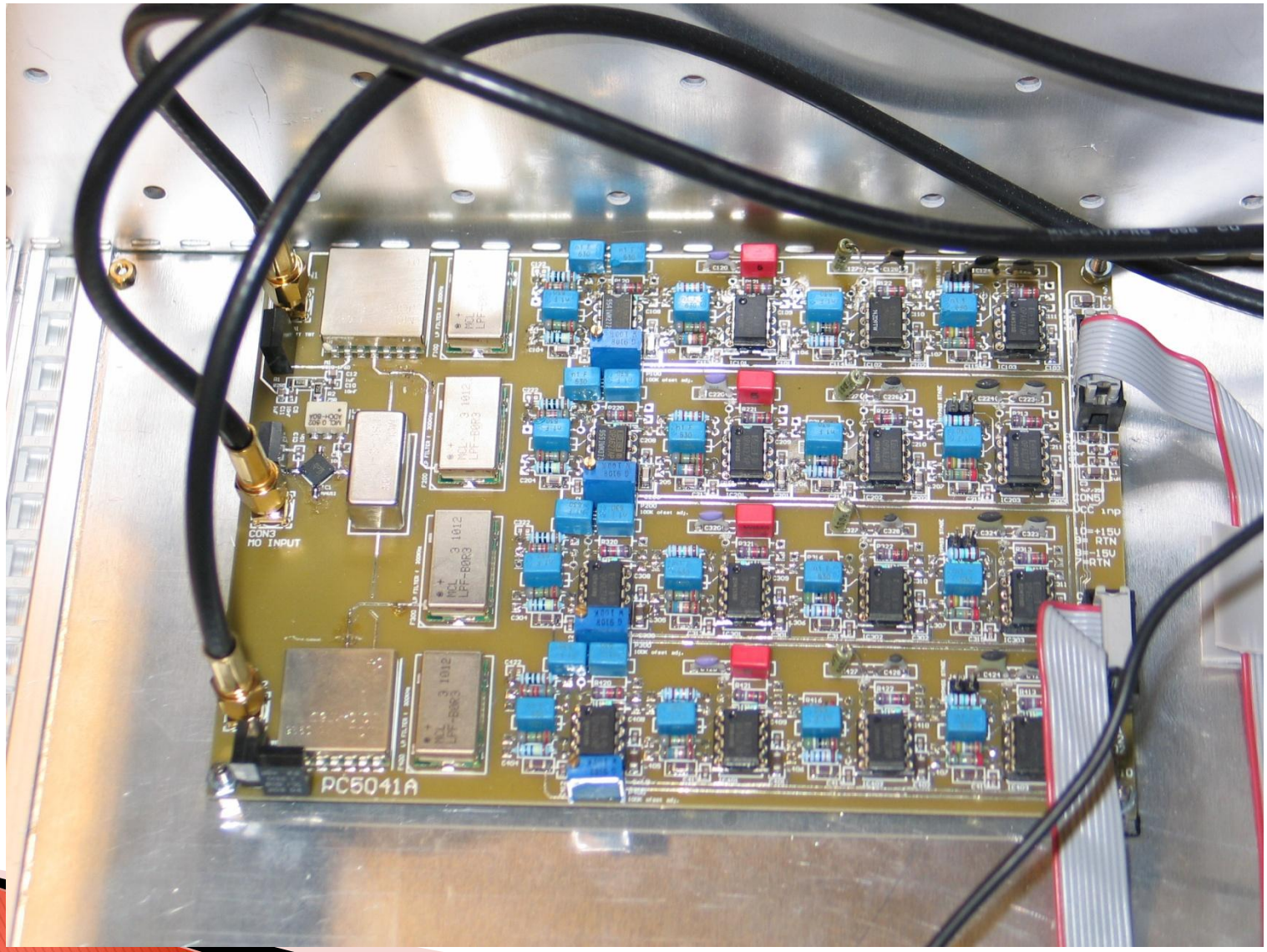
New ASTRIDx LLRF

- We are currently making a new LLRF for ASTRID
  - Same system to be used for ASTRID2
- Digital control of baseband signal
  - Detection: IQ demodulators with low pass filter
    - ±180° phase detection
  - Control: Amplitude and Phase (voltage controlled)
  - A computer (PC) running LabVIEW Real-Time with FPGA equipped multifunction card to measure and control the baseband signals
    - NI PCIe-7852R:
      - Virtex 5 FPGA, 8 AI, 750 kS/s/ch, 8 AO, 1 MS/s/ch, 16 bit
  - Amplitude Loop is implemented on the FPGA
  - Tuning Loop and Phase Loop will be implemented in the Real-Time program

ASTRIDx LLRF implementation

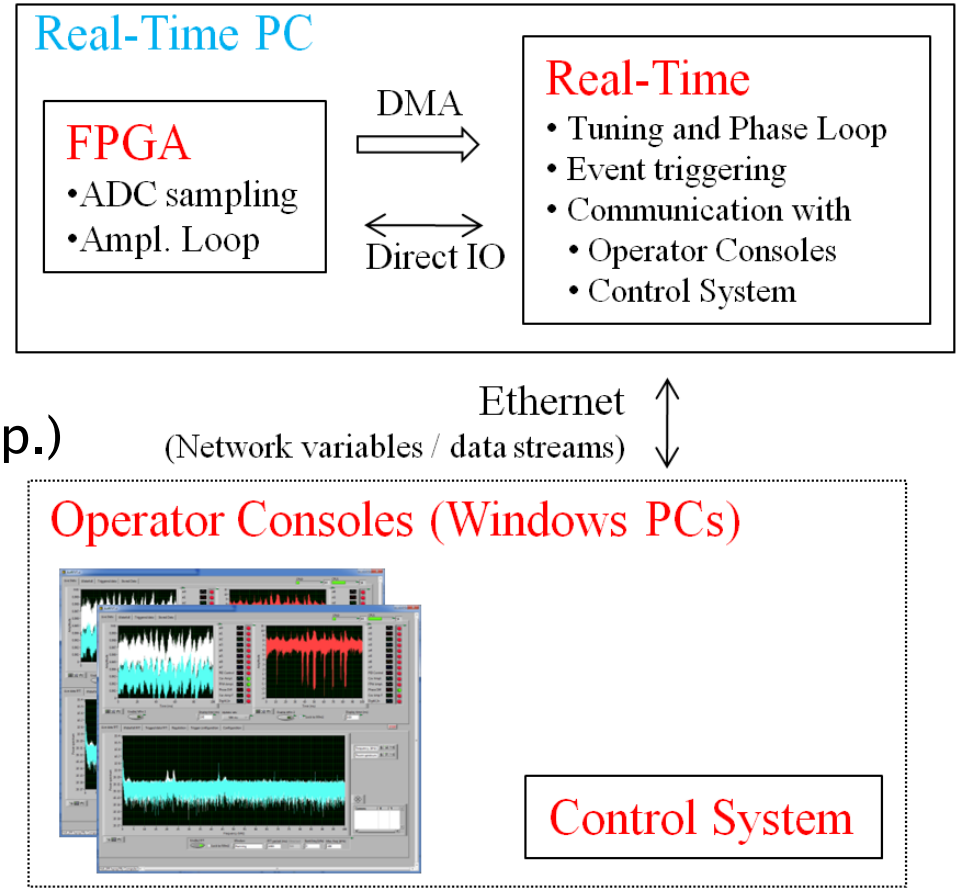


IQ demodulators (2 channels)
with 100 kHz lowpass filter

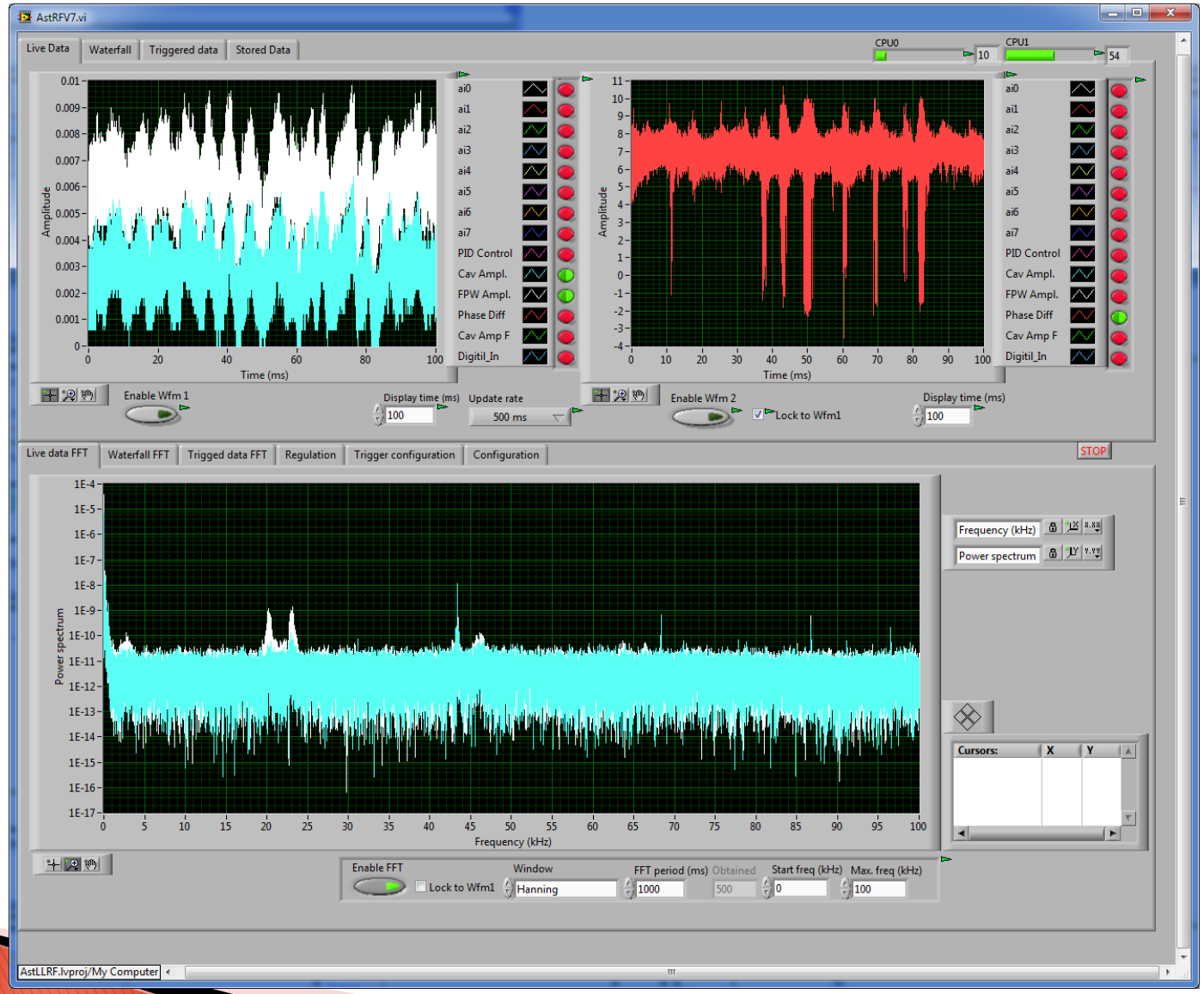


System with 3 LabVIEW programs

- FPGA
  - Data acquisition (8 channels, 500 kS/s)
    - Data are transferred via DMA to Real-Time program
  - Amplitude Loop
- Real-Time
  - Tuning and Phase Loop
  - Event Triggering (store interesting events)
  - Communicate with
    - Display Program (Host App.)
    - Control System
- Host Application
  - Operator Console
  - Displays the data
  - FFT for waterfall plot



Screendump of LLRF program



Experience with LabVIEW FPGA

- Much easier than VHDL (for us)
- But still need to understand FPGA details
- LabVIEW environment was not stable enough
  - LabVIEW 2009 SP1: PID toolkit often made FPGA compilation fail
    - Solved in LabVIEW 2010
  - Examples was not quite good enough
- We underestimated the development time!
  - More complex than expected
    - Long compile time slowed down development

Status of LLRF

- Currently prototyping RF parts
  - Have a working IQ demodulator
  - Testing voltage controlled attenuator
- Software
  - FPGA program is fully working
    - Acquisition with DMA to Real-Time
    - Amplitude Loop
  - Real-Time is basically finished
    - Missing tuning and phase loop
  - Host application is basically working
- First test of closed amplitude loop with beam successful
- We expect to bring the system into operation in December