NEW HIGH VOLTAGE CONTROL SYSTEM FOR BIMORPH BENDING MIRRORS PERFORMANCE AND APPLICATIONS

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DIGITAL POWER SUPPLY CONTROLLER

The power supply system used to drive this mirror is composed by a 3U high rack containing four output cards with four high voltage outputs each, one main controller board and one power supply board. The main controller board is connected via Ethernet to a rugged industrial computer interfaced to any computer of a Local Area Network (Wi-Fi or Ethernet). All four high voltage outputs are terminated with standard high voltage SHV connectors. There are two more SHV connectors for adjacent channel hardware daisy chain protection, as mirrors have stringent electric specifications on adjacent channels. All connections come from a backplane carrying all needed signals to the boards installed. Controlling commands can be issued through a LabVIEW™ client or some of the most popular synchrotron facility control systems (Epics, Tango). System control can also be done through a web page.

AD/DA CONVERSION

Voltage monitoring is achieved by sensing the real outputs of all four channels after high stability, high voltage resistive dividers and feeding four true 24-bit delta-sigma ADC converters. The effective resolution of this converter for full speed conversion rates goes down to 19-bit, which allows grabbing 16-bit noise free data. These values are then loaded to the DSP and processed with a PID algorithm. The regulation outputs of the PID controller are then sent to the four 16-bit DAC converters closing the loop.

DIGITAL CONTROLLER

The heart of the system is a Texas TMS320F2808 100MHz DSP mounted on each output card. It performs the digital control of the four channels included on the board. One eeprom memory keeps all calibration data of the high voltage channels on board. A cubic polynomial has been used to correct the non linearity of the high voltage resistive dividers with respect to the working voltage. Four coefficients are used to get the best fit of the voltage readout. On this memory there is plenty of room to put other coefficients in order to increase the order of the polynomial or to use other methods like look up tables. Main program is written in the internal DSP flash memory, automatically loaded into its fast ram memory to speed up operation and work at full power. The firmware is completely written in C-code. All the devices controlled by the DSP (like ADCs, DACs, Eeprom) have a serial SPI interface working at a speed of 8MHz, thus taking not more than 2us time to transfer 16-bit data.
The regulator is a standard PID controller with anti-windup.
The discrete control equation is: $u(k)=u_p(k)+u_i(k)+u_d(k)$ where:

1) $u_p(k)$ is the proportional part, $u_p(k)=K_p\, e(k)$ (e(k) is the error variable)
2) $u_i(k)$ is the integral part, $u_i(k)=K_i \sum_{i=0,k} [e(i)]$
3) $u_d(k)$ is the derivative part, $u_d(k)=K_d[e(k)-e(k-1)]$

V_{err} is computed as the difference between V_{ref} (set point) and V_{out}, so the proportional output is simply evaluated as $V_p=K_p*V_{err}$.
The integral part is computed as $V_i=V_{i-1}+(K_i*V_p)+(K_c*V_{saterr})$ where the last addendum is the anti windup term. This value is evaluated as the difference between the output value after and before limiter. The derivative part is simply $V_d=K_d*(V_p-V_{p-1})$.

The digital control loop is working at 40 kHz ensuring enough bandwidth for this application, as the mirror itself has a limited bandwidth, and higher frequency components of the driving voltage are intrinsically rejected. Further developments will insure increasing the bandwidth of the controller by using faster SPI devices (higher data rate), and recoding some time crucial parts of the firmware directly in assembler.

RESULTS

Figure 1 shows the block diagram of the power supply. Both rails are controlled by the DSP via a D/A converter, in order to get adaptive voltage settings. This means that there is no need to keep the negative rail up to its maximum voltage and dissipate energy while the output is completely positive. The maximum drain and source capabilities are fixed up to 500uA per channel

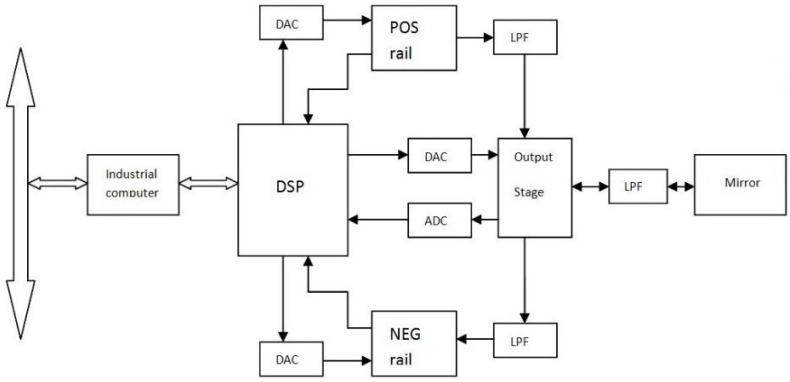

Figure 1

On a 2kV bipolar module the maximum resolution achieved for a set voltage is about 60mV.Actual noise and residual peak values at the output of these modules are better than 15ppm/FS and their long term stability is better than 100ppm/FS. These results can be improved by filtering the outputs.

If the system is thermo-statised, stability improves. Metrology and experimental results in laboratory with a long trace profiler in a thermo-statised (0.2C/week) room have shown medium and long term stability improved by a factor of two. After a week of applying the same voltage at the electrodes, the same profile (within the LTP sensibility) was measured.

REFERENCES

[1] R. Signorato, T. Ishikawa, "R&D on third generation multi-segmented piezoelectric bimorph mirror substrates at Spring-8", *NIMA :13168 - Nuclear Instruments and Methods in Physics Research A 0 (2001) pag 1–4*

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